

Patent

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Docket No. 10231-US-PA  
Application No.: 10/605,034

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Applicant : Tao et al.  
 Application No. : 10/605,034  
 Filed : September 3, 2003  
 For : CHIP PACKAGE STRUCTURE AND METHOD FOR  
 MANUFACTURING THE SAME  
 Art Unit : 2814  
 Examiner : HA, NATHAN W.

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Assistant Commissioner for Patent  
Alexandria, VA 22314

In response to the Notice of Appeal filed on August 8, 2005, please find the *Appeal Brief* in 12 pages.

Please charge the payment in the amount of US\$500 to account No. 50-2620 (Order No.: 10231-US-PA) to cover the fee set forth in 37 CFR 1.17(c) for filing an Appeal Brief.

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Thank you for your assistance in the subject matter. If you have any questions, please feel free to contact me.

Respectfully Submitted,  
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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

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**EX PARTE TAO et al.**

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**Application for Patent**

**Filed September 03, 2003**

**Serial No. 10/605,034**

**FOR:**

**CHIP PACKAGE STRUCTURE WITH STIFFENER AND  
METHOD FOR MANUFACTURING THE SAME**

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**APPEAL BRIEF**

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USSN 10/605,034

USSN 10/605,034

Appeal Brief

## TABLE OF CONTENTS

	<u>Page No.</u>
I. Real party in interest.....	1
II. Related appeals and interferences.....	1
III. Status of the claims.....	1
IV. Status of amendments.....	1
V. Summary of claimed subject matter .....	1
VI. Grounds of rejection to be reviewed on appeal .....	2
<i>Were claims 1, 3, 5, 7-9 and 11-13 properly rejected under 35 U.S.C. 102(e) as being anticipated by Zhao? .....</i>	<i>2</i>
<i>Was claim 4 properly rejected under 35 U.S.C. 103(a) as being obvious over Zhao in view of Wang? .....</i>	<i>2</i>
<i>Was claim 6 properly rejected under 35 U.S.C. 103(a) as being obvious over Zhao? .....</i>	<i>2</i>
<i>Were claims 14-16 and 18-19 properly rejected under 35 U.S.C. 103(a) as being obvious over Zhao? .....</i>	<i>2</i>
VII. Arguments .....	3
A. The related law .....	3
B. Grouping of the claims .....	4
C. <i>Claims 1, 3, 5, 7-9 and 11-13 were improperly rejected under 35 U.S.C. 102(e) as being anticipated by Zhao. .....</i>	<i>4</i>
D. <i>Claim 4 was improperly rejected under 35 U.S.C. 103(a) as being obvious over Zhao in view of Wang. ....</i>	<i>6</i>
E. <i>Claim 6 was improperly rejected under 35 U.S.C. 103(a) as being obvious over Zhao. ....</i>	<i>7</i>
F. <i>Claims 14-16 and 18-19 were improperly rejected under 35 U.S.C. 103(a) as being obvious over Zhao. ....</i>	<i>8</i>
G. Conclusion .....	9
VIII. Claims appendix .....	10

**I. Real party in interest**

The real party in interest is Advanced Semiconductor Engineering, Inc., the assignee of record.

**II. Related appeals and interferences**

There are no related appeals and/or interferences.

**III. Status of the claims**

A total of 23 claims were presented during prosecution of this application. Claims 2, 10, 17 and 20-23 have been cancelled. Applicant appeals rejected claims 1, 3-9, 11-16 and 18-19 from the Examiner's final rejection.

**IV. Status of amendments**

A proposed amendment was filed by applicants on November 11, 2004, proposing amendments to the specification (paragraph [0017]), the title and claims. In the Final Office Action dated March 08, 2005, the proposed amendment filed on November 11, 2004 was entered. No amendment to the claim was filed after the Final Rejection.

**V. Summary of claimed subject matter**

The present invention provides a chip package structure process. The process comprises disposing a plurality of chips on a matrix substrate and disposing a stiffener on the matrix substrate, wherein the stiffener includes an outer surface and an opposite inner surface and the inner surface of the stiffener faces the matrix substrate, and the stiffener has a plurality of openings and the chips are completely exposed by the openings of the stiffener. A molding compound is formed to cover the chip, the matrix substrate, the top surface and the bottom surface of the stiffener. The molding compound, the matrix substrate and the stiffener are diced to form a plurality of chip package structures. According to one embodiment, the stiffener is attached to the matrix substrate through an adhesive (Fig.3). Also in one

USSN 10/605,034

Appeal Brief

embodiment, a plurality of solder balls is formed on the matrix substrate before dicing the molding compound, the matrix substrate and the stiffener (Fig. 9).

The present invention provides a chip package structure, which comprises a substrate, a chip disposed on the substrate and electrically connected to the substrate, a stiffener disposed on the substrate and a molding compound. The stiffener includes an outer surface and an opposite inner surface and the inner surface of the stiffener faces the substrate, and the stiffener has at least an opening and the chip is completely exposed by the opening. The molding compound covers the chip, the substrate, the outer surface and the inner surface of the stiffener.

The present invention provides a chip package structure, which comprises a thin substrate, a chip disposed on the thin substrate and electrically connected to the thin substrate, a stiffener disposed on the thin substrate and a molding compound. The stiffener has at least an opening and the chip is completely exposed by the opening. The molding compound covers the chip, the thin substrate and the stiffener. The thin substrate has a thickness of between about 0.1mm and about 0.5 mm (paragraph [0028]).

Because the stiffener provides rigidity, warpage of the chip package structure is greatly reduced during the dicing process, even with the thin substrate. Through the support of the stiffener, the flatness of the chip package structure of the present invention is improved.

#### VI. Grounds of rejection to be reviewed on appeal

*Were claims 1, 3, 5, 7-9 and 11-13 properly rejected under 35 U.S.C. 102(e) as being anticipated by Zhao?*

*Was claim 4 properly rejected under 35 U.S.C. 103(a) as being obvious over Zhao in view of Wang?*

*Was claim 6 properly rejected under 35 U.S.C. 103(a) as being obvious over Zhao?*

*Were claims 14-16 and 18-19 properly rejected under 35 U.S.C. 103(a) as being obvious over Zhao?*

USSN 10/605,034

Appeal Brief

## VII. Arguments

## A. The related law

The standard for lack of novelty (i.e. anticipation) is one of strict identity. To anticipate a claim for a patent, a single prior source must contain all its essential elements.

*Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 U.S.P.Q. 81, 90 (Fed. Cir. 1986).

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. V. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference. .... These elements must be arranged as in the claim under review, ... but this is not an 'ipsissimis verbis' test. *In re Bond*, 910, F. 2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

The inquiry as to anticipation is symmetrical with the inquiry as to infringement of a patent. A classic test of anticipation provides : That which will infringe, if later, will anticipate, if earlier. *Knapp v. Morss*, 150 U.S. 221, 37 L. Ed. 1059, 14 S. Ct. 81 (1893); *Lindermann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1459, 221 U.S.P.Q. 481 (Fed. Cir. 1984). Therefore, by analogy, the all elements rule used for a determination of infringement finds its applicability in a determination of anticipation. Discussion of the all elements rule can be found in *Becton Dickinson and Co. v. C.R. Bard Inc.*, 17 U.S.P.Q. 2d 1962, 1967 (Fed. Cir 1989) and *Hi-Life Products Inc. v. American National Water-Mattress Corp.*, 6 U.S.P.Q.2d 1132, 1133 (Fed. Cir. 1988).

A prima facie case of obviousness requires that the reference teachings "appear to have suggested the claimed subject matter." *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143, 147 (CCPA 1976). To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

USSN 10/605,034

Appeal Brief

When more than one reference or source of prior art is required in establishing the obviousness rejection, "it is necessary to ascertain whether the prior art teachings would appear to be sufficient to one of ordinary skill in the art to suggest making the claimed substitution or other modification." *In re Lalu*, 747 F.2d 703, 223 USPQ 1257, 1258 (Fed. Cir. 1984). There must be some motivation to combine the references; this motivation must come from "the nature of the problem to be solved, the teachings of the prior art, [or] the knowledge of persons of ordinary skill in the art." *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998).

Finally, if an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d, 1596 (Fed. Cir. 1988).

B. Grouping of the claims

For the ground of rejection contested by appellant in this appeal, claims 1, 3-9 and 11-13 may be treated as one group to stand or fall together, and claims 14-16 and 18-19 may be treated as one group to stand or fall together. Independent claims 1 and 14 may be taken as representatives for the issue on appeal.

C. *Claims 1, 3, 5, 7-9 and 11-13 were improperly rejected under 35 U.S.C. 102(e) as being anticipated by Zhao.*

1. The rejection

The Final Office Action, dated March 08, 2005, rejected claims 1-3, 5 and 7-13 under 35 USC §102(e) as anticipated by Zhao et al. (U.S. Publication No. 2003/0179556; hereinafter "Zhao") (Final Office Action, pages 2-3). However, claims 2 and 10 had been cancelled according to the amendment filed on November 11, 2004. Therefore, appellant assumes this 102 rejection directed to claims 2 and 10 being clerical errors. In making the above rejections, the Examiner has construed Zhao to disclose the chip package structure process. The Final Office Action stated that "Zhao discloses a chip package structure process, comprising: providing a matrix substrate 104; disposing a plurality of chips 102....; disposing a stiffener 112 on the matrix substrate....". The Office Action further asserted that "...the stiffener has a plurality of openings. Fig. 20i, step 2032, and the chip are completely exposed by the openings".

USSN 10/605,034

Appeal Brief

However, as explained in greater detail subsequently, the interpretation and reasons relied on by the Examiner are respectfully believed to be incorrect.

2. The prior art

Zhao discloses a flex BGA package 110, wherein stiffener 112 is laminated to the surface of the substrate 104, and an IC die 102 is mounted on the surface of the stiffener 112 (Figs. 1b-4, [0057]). In Zhao's Figure 20i, step 2032, it teaches that "a second opening is formed in the stiffener that substantially coincides with the first opening to expose a portion of the surface of the first substrate.".

3. The prior art differentiated

In order to properly anticipate Applicant's claimed invention under 35 U.S.C §102, each and every element of the claims in issue must be found, "either expressly or inherently described, in a single prior art reference." "The identical invention must be shown in as complete detail as contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Applicants submit that independent claims 1 and 9 patently define over the prior references for at least the reason that the cited art fails to disclose each and every feature as claimed in the present invention.

Claims 1 and 9 teach, among other things, "...disposing a stiffener on the matrix substrate, wherein the stiffener includes an outer surface and an opposite inner surface and the inner surface of the stiffener faces the matrix substrate, and wherein the stiffener has a plurality of openings and the chips are completely exposed by the openings of the stiffener...". Contrary to the Office's assertion, Zhao does not teach or disclose the above-mentioned claimed features. Clearly, from Zhao's figures and teachings, Zhao's IC die 102 is mounted on the surface of the stiffener 112 (Figs. 1b-4, [0057]), but not at all exposed by the stiffener 112 or the opening of the stiffener 112. Although the stiffener of Zhao may also include a plurality of openings 114, those openings are arranged adjacent to all four sides of an IC die 102 mounting position 202 in the center of the stiffener 112 ([0058], Fig. 2A &2B). These openings in the stiffener of Zhao are formed to allow for wire bonds 108 to connect IC die to the substrate. In Figure 20i, step 2032, Zhao teaches forming a second opening in the stiffener that substantially coincides with the first opening to expose a portion of the surface of the first substrate, not to expose the chip completely. Since the openings in the stiffener

USSN 10/605,034

Appeal Brief

are formed adjacent to the disposition of the IC die 102, even if the stiffener is positioned above the die, the openings in the stiffener can not expose the die completely, let alone the fact that the stiffener taught by Zhao is formed below the die. Accordingly, Appellant respectfully submits that Zhao cannot possibly anticipate the claimed invention in this regard.

Accordingly, Zhao fails to teach or disclose all limitations as recited in the independent claims 1 and 9. Claims 3, 5, 7-8 and 11-13 depend from independent claims 1 and 9, and therefore are not anticipated by the reference Zhao for at least the reasons noted above, as well as for the additional features recited therein. In consequence, the rejections of claims 1, 3, 5, 7-9 and 11-13 were improperly rejected under 35 U.S.C. 102 as being anticipated by Zhao is submitted to be improper, and the Board is respectfully requested to cause these rejections to be withdrawn.

D. *Claim 4 was improperly rejected under 35 U.S.C. 103(a) as being obvious over Zhao in view of Wang.*

1. The rejection

The Final Office Action, dated March 08, 2005, rejected claims 4 and 20-23 under 35 USC 103(a) as being unpatentable over Zhao in view of Wang et al. (US Patent No. 5,977,626, hereinafter "Wang"). However, claims 20-23 had been cancelled according to the amendment filed on November 11, 2004. Therefore, appellant assumes this 103 rejection directed to claims 20-23 again being clerical errors. The Examiner has construed Zhao to disclose the chip package structure process except the stiffener being attached to the substrate through an adhesive layer. The Examiner cited Wang to teach the lacking feature.

2. The prior art

Zhao discloses a flex BGA package 110, wherein stiffener 112 is laminated to the surface of the substrate 104, and an IC die 102 is mounted on the surface of the stiffener 112 (Figs. 1b-4, [0057]). In Zhao's Figure 20i, step 2032, it teaches that "a second opening is formed in the stiffener that substantially coincides with the first opening to expose a portion of the surface of the first substrate."

USSN 10/605,034

Appeal Brief

Wang discloses a heat spreader or heat slug 32 being arranged over the top surface (first major surface) of the substrate 20 by using adhesive material 34 (Fig. 2; col. 3, lines 49-51).

### 3. The prior art differentiated

As discussed above, Zhao's the chip is not completely exposed by the stiffener or the openings of the stiffener, whereas the chip of the present invention is completely exposed by the opening(s) of the stiffener. Therefore, even if the heat sink is secured to the substrate by the adhesive, the whole process, having the die being mounted to the stiffener and not completely exposed by the stiffener, is still different from the present invention.

Accordingly, Appellant respectfully submits to the Board that the teachings of Zhao and Wang are deficient in rendering claim 4 unpatentable.

### E. *Claim 6 was improperly rejected under 35 U.S.C. 103(a) as being obvious over Zhao.*

#### 1. The rejection

The Final Office Action, dated March 08, 2005, rejected claim 6 under 35 USC 103(a) as being unpatentable over Zhao. However, the detailed rejections by the Examiner was directed to the previously cited prior art Nakayama (US Publication No. 2003/0164549; hereinafter "Nakayama"). The Examiner cited Nakayama for teaching the solder balls being formed before dicing the molding compound.

#### 2. The prior art

Zhao discloses a flex BGA package 110, wherein stiffener 112 is laminated to the surface of the substrate 104, and an IC die 102 is mounted on the surface of the stiffener 112 (Figs. 1b-4, [0057]). In Zhao's Figure 20i, step 2032, it teaches that "a second opening is formed in the stiffener that substantially coincides with the first opening to expose a portion of the surface of the first substrate.".

Nakayama discloses positioning a plurality of external electrodes 52 on the substrate 10 (Fig. 4) before the step of dicing the semiconductor device 1 ([0084]).

USSN 10/605,034

Appeal Brief

3. The prior art differentiated

As discussed above, Zhao's the chip is not completely exposed by the stiffener or the openings of the stiffener, whereas the chip of the present invention is completely exposed by the opening(s) of the stiffener. Still, Nakayama fails to remedy the deficiency of Zhao. Even considering the combination of Zhao and Nakayama, it can not arrive at the present invention.

Accordingly, Appellant respectfully submits to the Board that the teachings of Zhao and Nakayama are deficient in rendering claim 6 unpatentable.

F. *Claims 14-16 and 18-19 were improperly rejected under 35 U.S.C. 103(a) as being obvious over Zhao.*

1. The rejection

The Final Office Action, dated March 08, 2005, rejected claims 14-6 and 18-19 under 35 USC 103(a) as being unpatentable over Zhao. Similarly, appellant assumes this 103 rejection directed to claims 14-6 being clerical errors and this 103 rejection should be directed to claims 14-16. The Examiner has construed Zhao to disclose the chip package structure except the thickness of the substrate. The Office Action further contended that "it would be obvious to one person of ordinary skill in the art to modify the thickness of the substrate because applicant has not disclosed that this thickness provides an advantage, is used for a particular purpose, or solve a stated problem."

2. The prior art

Zhao discloses a flex BGA package 110, wherein stiffener 112 is laminated to the surface of the substrate 104, and an IC die 102 is mounted on the surface of the stiffener 112 (Figs. 1b-4, [0057]). In Zhao's Figure 20i, step 2032, it teaches that "a second opening is formed in the stiffener that substantially coincides with the first opening to expose a portion of the surface of the first substrate.".

3. The prior art differentiated

As discussed above, from Zhao's figures and teachings, Zhao's IC die 102 is mounted on the surface of the stiffener 112 (Figs. 1b-4, [0057]), but not at all exposed by the

USSN 10/605,034

Appeal Brief

stiffener 112 or the opening of the stiffener 112. Although the stiffener of Zhao may also include a plurality of openings 114, those openings are arranged around four sides of IC die 102 and the die 102 is not completely exposed by the openings 114. Accordingly, appellant respectfully submits that the structure of the present invention is patentably distinct from the prior art reference because Zhao fails to disclose or suggest all limitations of claim 14.

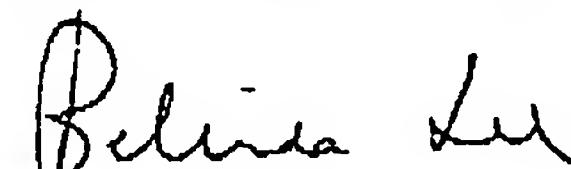
As admitted by the Examiner, Zhao fails to disclose the thickness of the substrate. However, even if modified Zhao's substrate for the thickness range, such modification of Zhao's structure is still different from that of this invention. Therefore, it is respectfully submitted that claim 14 is not obvious over Zhao and dependent claims 15-16, 18-19 patentably distinguish over Zhao, for at least the reasons stated above as well as for the additional features that these claims recite. Reconsideration and withdrawal of these 103 rejections are respectfully requested.

G. Conclusion.

As noted, the Examiner has not properly applied 35 U.S.C. § 102 and 35 U.S.C. § 103, and his rejection of the claims at issue. As such, Applicants believe that the rejections under 35 U.S.C. § 102 and 35 U.S.C. § 103 to be in error, and respectfully request the Board of Appeals and interferences to reverse the Examiner's rejections of the claims on appeal.

Date : Oct. 6, 2005

Respectfully submitted,

  
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USSN 10/605,034

Appeal Brief

**VIII. Claims appendix****CLAIMS ON APPEAL:**

Claim 1. (previously presented) A chip package structure process, comprising:  
providing a matrix substrate;

disposing a plurality of chips on the matrix substrate and the chips are electrically connected to the matrix substrate;

disposing a stiffener on the matrix substrate, wherein the stiffener includes an outer surface and an opposite inner surface and the inner surface of the stiffener faces the matrix substrate, and wherein the stiffener has a plurality of openings and the chips are completely exposed by the openings of the stiffener;

providing a molding compound to cover the chips, the matrix substrate, the outer surface and the inner surface of the stiffener; and

dicing the molding compound, the matrix substrate and the stiffener to form a plurality of chip package structures.

**Claim 2. (cancelled)**

Claim 3. (original) The chip package structure process of claim 1, wherein the inner surface of the stiffener faces the chips.

Claim 4. (original) The chip package structure process of claim 1, wherein the stiffener is attached to the matrix substrate through an adhesive.

Claim 5. (original) The chip package structure process of claim 1, wherein a plurality of solder balls are formed on the matrix substrate after dicing the molding compound, the matrix substrate and the stiffener.

Claim 6. (original) The chip package structure process of claim 1, wherein a plurality of solder balls are formed on the matrix substrate before dicing the molding compound, the matrix substrate and the stiffener.

USSN 10/605,034

Appeal Brief

**Claim 7. (original)** The chip package structure process of claim 1, wherein the chips are attached to the matrix substrate through an adhesive in the step of disposing the plurality of chips and a plurality of wires are formed by wire-bonding to electrically connect the chips and the matrix substrate.

**Claim 8. (original)** The chip package structure process of claim 1, wherein a material of the stiffener is copper.

**Claim 9. (previously presented)** A chip package structure, comprising:

a substrate;

a chip, disposed on the substrate and electrically connected to the substrate;

a stiffener, disposed on the substrate, wherein the stiffener includes an outer surface and an opposite inner surface and the inner surface of the stiffener faces the substrate, and wherein the stiffener has at least an opening and the chip is completely exposed by the opening; and

a molding compound, covering the chips, the matrix substrate, the outer surface and the inner surface of the stiffener.

**Claim 10. (cancelled)**

**Claim 11. (original)** The chip package structure of claim 9, wherein the inner surface of the stiffener faces the chip.

**Claim 12. (original)** The chip package structure of claim 9, wherein the chip package structure further includes a plurality of wires and the chip disposed on the substrate is electrically connected to the substrate through the wires.

**Claim 13. (original)** The chip package structure of claim 9, wherein a material of the stiffener is copper.

USSN 10/605,034

Appeal Brief

**Claim 14. (previously presented) A chip package structure, comprising:**

**a thin substrate, wherein the thin substrate has a thickness of between about 0.1mm and about 0.5 mm;**

**a chip, disposed on the thin substrate and electrically connected to the thin substrate;**

**a stiffener, disposed on the thin substrate, and wherein the stiffener has at least an opening and the chip is completely exposed by the opening; and**

**a molding compound, covering the chips, the thin substrate and the stiffener.**

**Claim 15. (original) The chip package structure of claim 14, wherein the stiffener includes an outer surface and an opposite inner surface and the inner surface of the stiffener faces the thin substrate and the molding compound covers the inner surface and the outer surface of the stiffener.**

**Claim 16. (original) The chip package structure of claim 14, wherein the inner surface of the stiffener faces the chip.**

**Claim 17. (cancelled)**

**Claim 18. (original) The chip package structure of claim 14, wherein the chip package structure further includes a plurality of wires and the chip disposed on the substrate is electrically connected to the substrate through the wires.**

**Claim 19. (original) The chip package structure of claim 14, wherein a material of the stiffener is copper.**

**Claims 20-23. (cancelled)**